COURSE SCHEME
EXAMINATION SCHEME
ABSORPTION SCHEME
&
SYLLABUS

Of

First, Second, Third & Fourth Semester
Choice Base Credit System (CBCS)
Of
Master of Technology (M.Tech)

In

Embedded System and Computing
Of
RASHTRASANT TUKDOJI MAHARAJ
NAGPUR UNIVERSITY, NAGPUR

Rashtrasant Tukdoji Maharaj Nagpur University, Nagpur
Faculty of Engineering & Technology
Course and Examination Scheme of Master of Technology
Choice Base Credit System(CBCS)

I Semester M. Tech. Embedded System and Computing (ESC)

Subject Code	Subject	Teaching Scheme			Examination Scheme								
					Theory					Practical			
		Hours per week		No. of Credits	Duration of Paper (Hrs.)	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks
		L	P			University Assessment	College Assessment			University Assessment	College Assessment		
PGESC101T	Microcontroller for Embedded System Design	4	-	4	3	70	30	100	50	-	-	-	-
PGESC102T	Embedded System Concepts	4	-	4	3	70	30	100	50	-	-	-	-
PGESC103T	High Performance Computer Architecture	4	-	4	3	70	30	100	50	-	-	-	-
PGESC104T	Elective –I (Discipline Specific)	4	-	4	3	70	30	100	50	-	-	-	-
PGOPEN105T	Elective –II (Open)	4	-	4	3	70	30	100	50	-	-	-	-
PGESC106P	Laboratory –I (MESD)	-	2	1	-	-	-	-	-	50	50	100	50
PGESC107P	Laboratory –II (ESC)	-	2	1	-	-	-	-	-	50	50	100	50
Total		20	4		-	350	150	500	-	100	100	200	-
Semester Total		24		22	700 Marks								

Elective –I (Discipline Specific) PGESC104/1T- **System Modeling and Simulation,** PGESC104/2T-**Distributed Embedded Systems**
Elective –II (Open) PGOPEN105/1T-**CMOS VLSI Design,** PGOPEN105/2T-**Soft Computing**

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Choice Base Credit System(CBCS)

II Semester M. Tech. Embedded System and Computing (ESC)

Subject Code	Subject	Teaching Scheme			Examination Scheme								
					Theory					Practical			
		Hours per week		No. of Credits	Duration of Paper (Hrs.)	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks
		L	P			University Assessment	College Assessment			University Assessment	College Assessment		
PGESC201T	Embedded System Programming	4	-	4	3	70	30	100	50	-	-	-	-
PGESC202T	Real Time Operating System for Embedded System	4	-	4	3	70	30	100	50	-	-	-	-
PGESC203T	Advance Digital Image Processing	4	-	4	3	70	30	100	50	-	-	-	-
PGESC204T	Elective –III (Discipline)	4	-	4	3	70	30	100	50	-	-	-	-
PGFD205T	Foundation Courses -I	4	-	4	3	70	30	100	50	-	-	-	-
PGESC206P	Laboratory –III (ESP)	-	2	1	-	-	-	-	-	50	50	100	50
PGESC207P	Laboratory –IV (ADIP)	-	2	1	-	-	-	-	-	50	50	100	50
Total		20	4		-	350	150	500	-	100	100	200	-
Semester Total		24		22	700 Marks								

Elective –III (Discipline Specific) PGESC204/1T-**Intelligent Embedded System,** PGESC204/2T- P**rinciples of Embedded Networked System Design**
Foundation Courses –I PGFD205T **-Research Methodology**

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III Semester M. Tech. Embedded System and Computing (ESC)

Subject Code	Subject	Teaching Scheme			Examination Scheme								
					Theory					Practical			
		Hours per week		No. of Credits	Duration of Paper (Hrs.)	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks
		L	P			University Assessment	College Assessment			University Assessment	College Assessment		
PGOPEN301T	Elective –IV (Open)	4	-	4	3	70	30	100	50	-	-	-	-
PGFD302T	Foundation Courses –II	4	-	4	3	70	30	100	50	-	-	-	-
PGESC303P	Project Seminar	-	-	8	-	-	-	-	-	-	200	200	100
Total		8	-	-		140	60	200	-	-	200	200	-
Semester Total		8		16	400 Marks								

Elective –IV (Open) PGOPEN301/1T- **Designing Embedded Communication Software,** PGOPEN301/2T- **Embedded System Testing and Verification**
Foundation Courses –II PGFD302T **-Project planning and Management**

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IV Semester M. Tech. Embedded System and Computing (ESC)

Subject Code	Subject	Teaching Scheme			Examination Scheme								
					Theory					Practical			
		Hours per week		No. of Credits	Duration of Paper (Hrs.)	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks
		L	P			University Assessment	College Assessment			University Assessment	College Assessment		
PGESC401P	Project	-	-	16	-	-	-	-	-	400	-	400	200
Total		-	-		-	-	-	-	-	400	-	400	-
Semester Total		-		16	400 Marks								

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Course and Examination Scheme of Master of Technology
Choice Base Credit System (CBCS)

Absorption Scheme

Proposed Scheme of Absorption of Old course to New course of First to Fourth Semesters

I Semester M. Tech. (ESC)

Table 1

Subject Code (OLD)	Subject (OLD)		Subject Code (NEW)	Subject (NEW)	
PG-ES1-01	Micro Controllers For Embedded System Design		PGESC101T	Microcontroller for Embedded System Design	
PG-ES1-02	Embedded System Concepts		PGESC102T	Embedded System Concepts	
PG-ES1-03	Advanced Computer Architecture		PGESC103T	High Performance Computer Architecture	
PG-ES1-04-01	Object Oriented Systems (Elective–I)		---	---	
PG-ES1-04-02	Function/Architecture Optimization & co-design of Embedded systems (Elective–I)		---	---	
PG-ES1-04-03	CPLD And FPGA Architecture And Applications (Elective–I)		---	---	
PG-ES1-05-01	Soft Computing (Elective-II)		PGOPEN105/2T	Elective–II (Open) Soft Computing	
PG-ES1-05-02	Mobile Computing (Elective-II)		---	---	
PG-ES1-05-03	System Modeling & Simulation (Elective–II)		---	---	
PG-ES1-06	Computer System Lab-1		---	---	
PG-ES1-07	Seminar-I		---	---	

Table 2

Subject Code (NEW)	Subject (NEW)		Subject Code (OLD)	Subject (OLD)	Remark
PGESC101T	Microcontroller for Embedded System Design		PG-ES1-01	Micro Controllers For Embedded System Design	PG-ES1-01 Not Clear Have to appear New PGESC101T
PGESC102T	Embedded System Concepts		PG-ES1-02	Embedded System Concepts	PG-ES1-02 Not Clear Have to appear New PGESC102T
PGESC103T	High Performance Computer Architecture		PG-ES1-03	Advanced Computer Architecture	PG-ES1-03 Not Clear Have to appear New PGESC103T
PGESC104T	Elective–I (Discipline Specific)		---	---	Have to appear PGESC104T
PGOPEN105T	Elective–II (Open)		---	---	If you Have Clear old PG-ES1-05-01(Soft Computing) Then don't appear PGOPEN105T Otherwise Have to appear New PGOPEN105T Elective –II (OPEN)
PGESC106P	Laboratory –I (MESD)		---	---	Have to appear
PGESC107P	Laboratory –II (ESC)		---	---	Have to appear

Proposed Scheme of Absorption of Old course to New course of First to Fourth Semesters

II Semester M. Tech. (ESC)

Table 1

Subject Code (OLD)	Subject (OLD)		Subject Code (NEW)	Subject (NEW)	
PG-ES2-01	Advances in Algorithms		---------	----------	
PG-ES2-02	Real Time Operating System For Embedded System		PGESC202T	Real Time Operating System for Embedded System	
PG-ES2-03	Embedded Software Design		---------	----------	
PG-ES2-04-01	Wireless Communciations And Networks (Elective-3)		---------	----------	
PG-ES2-04-02	Intelligent Embedded Systems (Elective-3)		PGESC204/1T	Elective–III (Discipline) Intelligent Embedded System	
PG-ES2-04-03	Principles of Embedded Networked System Design (Elective-3)		PGESC204/2T	Elective–III (Discipline) Principles of Embedded Networked System Design	
PG-ES2-05-01	TCP/IP And Internet (Elective-4)		---------	----------	
PG-ES2-05-02	Satellite Communication (Elective-4)		---------	----------	
PG-ES2-05-03	Cryptography and Network Security		---------	----------	
PG-ES2-06	Computer System Lab-II		---------	----------	
PG-ES2-07	Seminar-II		---------	----------	
PG-ES2-08	Comprehensive Viva-Voce		---------	----------	

Table 2

Subject Code (NEW)	Subject (NEW)		Subject Code (OLD)	Subject (OLD)	Remark
PGESC201T	Embedded System Programming		---------	----------	Have to appear
PGESC202T	Real Time Operating System for Embedded System		PG-ES2-02	Real Time Operating System For Embedded System	PG-ES2-02 Not Clear Have to appear New PGESC202T
PGESC203T	Advance Digital Image Processing		---------	----------	Have to appear
PGESC204/1T	Elective–III (Discipline) Intelligent Embedded System		PG-ES2-04-02	Intelligent Embedded Systems (Elective-3)	PG-ES2-04-02 Not Clear Have to appear New PGESC204T
PGESC204/2T	Elective–III (Discipline) Principles of Embedded Networked System Design		PG-ES2-04-03	Principles of Embedded Networked System Design (Elective-3)	PG-ES2-04-03 Not Clear Have to appear New PGESC204T
PGFD205T	Foundation Courses -I		---------	----------	Have to appear
PGESC206P	Laboratory–III (ESP)		---------	----------	Have to appear
PGESC207P	Laboratory–IV (ADIP)		---------	----------	Have to appear

III Semester M. Tech. (ESC)

Table 1

Subject Code (OLD)	Subject (OLD)		Subject Code (NEW)	Subject (NEW)	
PG-ES3-01	Designing Embedded Communication Software		PGOPEN301/1T	Elective –IV (Open) Designing Embedded Communication Software	
PG-ES3-02	Distributed Embedded Systems & Computing		---	---	
PG-ES3-03	Seminar on Project Spade Work		PGESC303P	Project Seminar	

Table 2

Subject Code (NEW)	Subject (NEW)		Subject Code (OLD)	Subject (OLD)	Remark
PGOPEN301T	Elective –IV (Open)		PG-ES3-01	Elective –IV (Open) Designing Embedded Communication Software	If you Have Clear old PG-ES3-01 (Designing Embedded Communication Software) Then don't appear PGOPEN301T Otherwise Have to appear New PGOPEN301T Elective –IV (OPEN)
PGFD302T	Foundation Courses –II		---	---	Have to appear
PGESC303P	Project Seminar		PG-ES3-03	Project Seminar	If you Have Clear old PG-ES3-03 (Project Seminar) Then don't appear PGESC303P Otherwise Have to appear New PGESC303P Project Seminar

IV Semester M. Tech. (ESC)

Subject Code (OLD)	Subject (OLD)		Subject Code (NEW)	Subject (NEW)	
PG-ES4-01	Thesis & Defence		PGESC401P	Project	

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M. Tech. Embedded System and Computing (ESC) - I Semester

Course Code	Course	Teaching Scheme		
		Hours Per Week		Credits
		L	P	
PGESC101T	Microcontroller for Embedded System Design	4	-	4

UNIT I

INTRODUCTION TO EMBEDDED SYSTEMS

Review of Micro controllers and their Features. 8 & 16 Bit Micro Controller Families (of Intel 8051) Flash Series, Motorola 68HC11; Micro Chip PIC 16C6X and Micro controller hardware. Embedded RISC Processor Architectures – ARM6TDMI(Advanced RISC Machines).

UNIT II

MICRO CONTROLLER INTERFACING

8051, 68HC11, PIC-16C6X and ATMEL External Memory Interfacing – Memory Management Unit, Instruction and data cache, memory controller. On Chip Counters, Timers, Serial I/O, Interrupts and their use. PWM, Watch dog, ISP, IAP features.

UNIT III

PROGRAMMING

Instruction sets and assembly language programme concepts and programming the 8051, 68HC11, PIC-16C6X Micro controller ARM6TDMI Core (SOC) and PIC-IDE.

UNIT IV

Interrupt synchronization – Interrupt vectors & priority, external interrupt design. Serial I/O Devices –RS232 Specifications, RS422/Apple Talk/ RS 423/RS435 & other communication protocols. Serial communication controller, Ethernet Protocol, SDMA, Channels and IDMA Simulation.

UNIT V

CPM Interrupt controller and CPM Timers, Power controls, External BUS Interface system Development and Debugging.

CASE STUDIES: Design of Embedded Systems using the micro controller – 8051/ARM6TDMI, for applications in the area of Communications, Automotives, industrial control.

SUGGESTED BOOKS

1. M.A. Mazadi & J.G. Mazidi, “The 8051 Micro Controller & Embedded Systems”, Pearson Education. Asia (2000).
2. John B. Peatman, Designing with PIC Micro Controllers, Pearson Education.
3. Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 1999.
4. Cathey May and Silha 5. (Ed)., “The Power PC Architecture”, Morgan Kauffman Press (1998).

Course Code	Course	Teaching Scheme		
		Hours Per Week		Credits
		L	P	
PGESC102T	Embedded System Concepts	4	-	4

UNIT I: AN INTRODUCTION TO EMBEDDED SYSTEMS

An Embedded system, processor in the system, other hardware units, software embedded into a system, exemplary embedded systems, embedded system – on – chip (SOC) and in VLSI circuit.

UNIT II:

Processor and memory organization – Structural Units in a Processor, Processor selection for an embedded system, memory devices, memory selection for an embedded systems, allocation of memory to program cache and memory management links, segments and blocks and memory map of a system, DMA, interfacing
processors, memories and Input Output Devices.

UNIT III: DEVICES AND BUSES FOR DEVICE NETWORKS

I/O devices, timer and counting devices, serial communication using the "I2 C" CAN, profibus foundation field bus. and advanced I/O buses between the network multiple devices, host systems or computer parallel communication between the networked I/O multiple devices using the ISA, PCI, PCI-X and advanced buses.

UNIT IV: DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM

Device drivers, parallel port and serial port device drivers in a system, device drivers for internal programmable timing devices, interrupt servicing mechanism.

PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C, C++, VC++,AND JAVA:

Interprocess communication and synchronization of processes, task and threads, multiple processes in an application, problem of sharing data by multiple tasks and routines, interprocess communication.

UNIT V:

HARDWARE – software co-design in an embedded system, embedded system project management, embedded system design and co-design issues in system development process, design cycle in the development phase for an embedded system, use of target systems, use of software tools for development of an embedded system, use of scopes and logic analysis for system, hardware tests. Issues in embedded system design.

TEXTBOOK

1. Embedded systems: Architecture, programming and design by Rajkamal, TMH

REFERENCEs

1. Embedded system design by Arnold S Burger, CMP
2. An embedded software primer by David Simon, PEA
3. Embedded systems design: Real world design be Steve Heath; Butter worth Heinenann, Newton mass USA 2002
[1] 4. Data communication by Hayt.

Course Code	Course	Teaching Scheme		
		Hours Per Week		Credits
		L	P	
PGESC103T	High Performance Computer Architecture	4	-	4

Unit I

Introduction: review of basic computer architecture, Parallel Computer Models: The State of Computing, Multiprocessor and Multicomputer, Multivectors and SIMD Computers, PARAM and VLIS Models. Program and Network Properties: Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanism, System Interconnect Architecture,

Unit II

Principles of Scalable Performance: Performance Matrix and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches. Processor and Memory Hierarchy: Advanced Processor Technology, Super Scalar and Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.

Unit III

Bus, Cache and Shared Memory: Backplane Bus System, Cache Memory Organization, Shared Memory Organization, Sequential and Weak Consistency Model. Pipelining and Superscalar Techniques: Linear Pipeline Processors, Nonlinear Pipeline Processors, Instruction Pipeline Design, Arithmetic Pipeline Design, Super Scalar and Super pipeline Design

Unit IV

Multiprocessors and Multicomputer: Multiprocessor System Interconnects, Cache coherence and Synchronization Mechanism, Three Generations of Multicomputer, Message Passing Mechanism. Multivector and SIMD Computers: Vector Processing Principle, Multivector Multiprocessors, Compound vector Processing, SIMD Computer Organization, The Connection Machine CM-5

Unit V

Scalable Multithreaded and Dataflow Architectures: Latency Hiding Techniques, Principles of Multithreading, Fine- Grain Multicomputer, Scalable and Multithread Architecture, Data Flow and Hybrid Architecture. Parallel Models, Recent trends in High performance computer architecture.

Text Books:

1. Kai Hwang, “Advanced Computer Architecture: Parallelism, Scalability, Programmability, McGraw Hill,1993

2. Kai Hwang and Faye A. Briggs, “Computer Architecture and Parallel Processing. McGraw, Hill,1985.

Reference Books:

1. D. A. Patterson & J. L. Hennessy, Computer Architecture – A Quantitative Approach, Morgan Kaufmann Publishers, 2nd edition – 1996.

Course Code	Course	Teaching Scheme		
PGESC104/1T	Elective –I (Discipline) **System Modeling and Simulation**	Hours Per Week		Credits
		L	P	
		4	-	4

UNIT I
Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT II
SIMULATION SOFTWARE: Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT III
BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT IV
MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

UNIT V
EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation.

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

TEXTBOOKS
1. System Modeling & Simulation, An Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modelling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCE BOOKS
1. Systems Simulation – Geoffery Gordon, PHI, 1978.

Course Code	Course	Teaching Scheme		
PGESC104/2T	Elective –I (Discipline) **Distributed Embedded System**	Hours Per Week		Credits
		L	P	
		4	-	4

Unit I : The Real Time Environment Overview Introduction, Functional Requirements, Temporal Requirements, Dependability Requirements, Classification of Real Time systems The Real Time systems Market, Examples of Real Time systems. Distributed System Overview System Architecture, Compensability, Scalability, Dependability Physical Installation.

Unit II : Global Time Overview Time and Order, Time Measurements, Dense Time versus sparse Time Internal Clock synchronization,

External clock synchronization

Unit III : Modeling Real Time Systems Appropriate Abstractions, The Structural Elements, Interfaces, Temporal Control, Worst case

Execution Time

Unit IV : Real Time Entities and Images Real time Entities, Real Time Image and Objects, Temporal accuracy, Permanence and

Idempotency. Fault Tolerance.

Unit V : The Time Triggered Protocol Introduction to TTP, Overview, Protocol Layers, Internal Operations of TTP/C, TTP/A for Field

Bus Applications, Advanced topic on distributed embedded system

Text Book

1. “Real Time Systems Design Principles for Distributed Embedded” Applications. By Herman Kopetz

Elective –II (Open)

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M. Tech. (ESC) - II Semester

Course Code	Course	Teaching Scheme		
		Hours Per Week		Credits
		L	P	
PGESC201T	Embedded System Programming	4	-	4

Unit I :
Introduction to Embedded Computing Overview, Characteristics of Embedding Computing Applications, Programming Embedded Systems Program Design Design Patterns for Embedded Systems Models of Program , Control and Data flow Graph.

Unit II :
Programming Languages Desired Language Characteristics, Introduction to Object Oriented Programming, Control, Multi tasking and Task Scheduling ,Timing Specifications, Run time Exception handling, Use of High Level Languages, C for Programming embedded systems, Object Oriented Programming for Embedded Systems in C++,

Unit III :
Java for Embedded Systems (J2ME) Overview, Developing J2ME applications, J2ME Configurations, J2ME Profiles, Setting
up development environment CLDC API

Unit IV :
Development using K JAVA GUI Components, Development using K Java Event Handling, MIDP API, CDS API.

Unit V :
J2ME for Mobile applications. Recent trend in embedded system programming

Text Book
1. Black Book of embedded programming in java

Course Code	Course	Teaching Scheme		
		Hours Per Week		Credits
		L	P	
PGESC202T	Real Time Operating System for Embedded System	4	-	4

Unit 1:

REVIEW OF OPERATING SYSTEMS - Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes – Introduction to Distributed operating system – Distributed scheduling.

Unit 2:

OVERVIEW OF RTOS RTOS Task and Task state - Process Synchronisation- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks

Unit 3:

REAL TIME MODELS AND LANGUAGES Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

Unit 4:

REAL TIME KERNEL Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

Unit 5:

RTOS APPLICATION DOMAINS RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

REFERENCES:

1. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.
2. Herma K., “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.
3 Charles Crowley, “Operating Systems-A Design Oriented approach” McGraw Hill 1997.
4 C.M. Krishna, Kang, G.Shin, “Real Time Systems”, McGraw Hill, 1997.
5. Raymond J.A.Bhur, Donald L.Bailey, “An Introduction to Real Time Systems”, PHI 1999. 6. Mukesh Sighal and N G Shi “Advanced Concepts in Operating System”, McGraw Hill

Course Code	Course	Teaching Scheme		
		Hours Per Week		Credits
		L	P	
PGESC203T	Advance Digital Image Processing	4	-	4

Unit 1:
Image Enhancement in the Spatial Domain: Spatial and Frequency methods, Basic gray level Transformations, Histogram Equalization, Histogram Processing, Local enhancement, Image Subtraction, Image Averaging, Basics of Spatial Filtering, Smoothing Spatial Filters, and Sharpening Spatial filters.

Unit 2:
Transforms: Introduction to the Fourier Transformation, Discrete Fourier Transformation, fast Fourier Transformation, Fourier Properties, 2D FT, Inverse Fourier Transform, Wavelet transform and multi resolution processing.

Unit 3:
Image Enhancement in the frequency Domain: Filtering in the Frequency Domain, Correspondence between filtering in the Spatial and Frequency Domain, Smoothing Frequency- Domain filters, Sharpening Frequency-Domain filters, Homomorphic Filtering, Implementation.

Unit 4:
Image Compression: Image Compression Models, Lousy & loss less compression, image compression standards. Image restoration, Color Image processing. Morphological Image Processing : Preliminaries, Dilation and Erosion, Opening and Closing, hit-or-miss Transformation, some Basic Morphological Algorithms, Extension to Gray-Scale Images.

Unit 5:
Image Segmentation: Point Detection, Line Detection, Edge detection, Gradient Operator, Edge Linking and Boundary Detection, Thrasholding, region-oriented Segmentation. Representation: Chain codes, Polygonal Approximations, Signatures, Boundary Segments. Skeleton of a Region Description: Boundary Descriptors, Shape Numbers, Fourier Descriptors, Regional Descriptors, Simple Descriptors, Topological Descriptors.

Text Books:

1. Rafael C. Gonzalez and Richard E. woods, “Digital Image processing” 2nd edition, Prentice Hall, 2002.
2. A. K. Jain, “Fundamentals of Digital Image Processing,” Prentice Hall
3. W. K. Pratt, “ Digital Image Processing”, 3rd Edition, John Wiley and sons, New York
4. Chanda Muzumdar, “Digital Image Processing”, Prentice Hall India.

Course Code	Course	Teaching Scheme		
PGESC204/1T	Elective –III (Discipline) **Intelligent Embedded System**	Hours Per Week		Credits
		L	P	
		4	-	4

UNIT I:-

Advances in Embedded Systems: Review of recent developments in embedded systems - systems on a chip (SoC), integration of IP cores, integrated microprocessor and programmable logic reconfigurable devices.

UNIT II:-

Identification of Existing Computational Intelligence Techniques: Identification of existing computational techniques such as neural networks and genetic algorithms. Advantages and disadvantages of an embedded systems implementation**.**

UNIT III:-

Requirements for re-configurable devices for plasticity, adaptation and autonomous self-organization. Interfacing, reliability and signal processing issues. Issues in the design and implementation of self-organizing intelligent embedded systems.

UNIT IV:-

Conventional and Bio-inspired Neural Networks: networks on an embedded system; embedded design, architectural and circuit configurations, efficient use of on-chip resources, on-chip and off-chip training issues; information coding approaches. Biologically plausible artificial implementations. Design and utilization of digital medium for implementations of neural networks; limitations and advantages of approach; performance and training issues.

UNIT V:

Research Developments: Recent advances in the design and implementation of intelligent embedded systems as implantable devices in animals and humans; hybrid biological and embedded silicon systems.

Reference Books:

1. G. Wilson, Embedded Systems and Computer Architecture, Oxford: Newnes, 2002.
2. W. Wolf, Computer as Components; Principles of Embedded Systems Design, Morgan Kaufmann, 2000.
3. T. Wilmhurst, The Design of Small Scale Embedded Systems, Palgrave, 2002.
4. J. Cooling, Software Engineering for Real-time Systems, Addison-Wesley, 2003.
5. W. Gerstner and W.M. Kistler, Spiking Neuron Models: Single Neurons, Populations, Plasticity, Cambridge University Press (August 2002), Paperback: ISBN 0 521 89079 9 : 40 USD.

Course Code	Course	Teaching Scheme		
		Hours Per Week		Credits
		L	P	
PGESC204/2T	Elective –III (Discipline) P**rinciples of Embedded Networked System Design**	4	-	4

UNIT I:

Embedded Network Systems, Representation of signals, Signal Propagation
Sensor Principles, Source detection and identification.

UNIT II:

Digital Communication, Multiple source estimation and multiple access communication
Networking, Network position & Synchronization services.

UNIT III:

Energy Management, Data Management, Articulation, Mobility, & infrastructure

UNIT IV:

Node Architecture, Network data integrity.

UNIT V:

Experimental system design, Ethical, legal and social implications of Ents
.Design Principles of ENS.

UNIT VI:

Application A: Gaussian Q function
Application B: Optimization

TEXT BOOK:

Principles of Embedded Networked System Design By Gregorg Poltic, William Kaiser

III Semester M. Tech. (SS)

Elective –IV (Open)

Foundation Course –II

Course Code	Course	Teaching Scheme		
		Hours Per Week		Credits
		L	P	
PGFD302T	**Project planning and Management**	4	-	4